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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/792,087	03/04/2004	Shinichi Kouzuma	OKI.462D	4887

7590 05/31/2005

VENABLE
Post Office Box 34385
Washington, DC 20043-9998

EXAMINER	
TRAN, ANH Q	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 05/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/792,087	KOUZUMA, SHINICHI	
	Examiner	Art Unit	
	Anh Q. Tran	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *26 and 27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *26* is/are rejected.

7)☒ Claim(s) *27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/073,022.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/4/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claim 26 is rejected under 35 U.S.C. 102(e) as being anticipated by Kogure et al (6,542,144).

Kogure shows a level shift circuit (101, Fig. 5) comprising:

a first transistor circuit (PFETs) which is conductive between a first node (C) and a first power supply line (GVDD) when a second node (B) is at a second power supply potential, and which is not conductive therebetween when said second node is at a first power supply potential;

a second transistor circuit (PFETs) which is conductive between said second node (B) and said first power supply line (GVDD) when said first node is at said second power supply potential, and which is not conductive therebetween when said first node is at said first power supply potential;

a third transistor circuit (NFET) which is conductive between said first node and a second power supply line (VSS) when an input signal (In) is at a first input potential, and

which is not conductive therebetween when said input signal is at a second input potential;

a fourth transistor circuit (NFET) which is conductive between said second node and said second power supply line when said input signal is at a second input potential, and which is not conductive therebetween when said input signal is at said first input potential; and

a fifth transistor circuit (Nch_TFT connected between node C and VSS) which switches a value of an inflow current or emission current of said second node or said first node according to a control signal (103, col. 8, lines 8-18), when said second node or said first node is conductive to both of said first power supply line and said second power supply line,

wherein said first transistor circuit comprises a first conductive type first transistor one end of which is connected to said first power supply line and a control terminal of which is connected to said second node, and a first conductive type second transistor one end of which is connected to an other end of said first transistor, an other end of which is connected to said first node, and a control terminal of which has said input signal provided thereto (the two PFET transistors serially connected between GVDD and node C),

said second transistor circuit comprises a first conductive type third transistor one end of which is connected to said first power supply line and a control terminal of which is connected to said first node, and a first conductive type fourth transistor one end of which is connected to an other end of said third transistor, an other end of which is

connected to said second node, and a control terminal of which has an inverted value of said input signal provided thereto (the two PFET transistors serially connected between GVDD and node B),

said third transistor circuit comprises a second conductive type fifth transistor one end of which is connected to said second power supply line, an other end of which is connected to said first node, and a control terminal of which has said input signal provided thereto (NFET transistor connected between node C and VSS), and

said fourth transistor circuit comprises a second conductive type sixth transistor one end of which is connected to said second power supply line, an other end of which is connected to said second node, and a control terminal of which has the inverted value (A) of said input signal provided thereto (NFET transistor connected between node B and VSS).

Allowable Subject Matter

3. Claim 27 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh Q. Tran whose telephone number is 571-272-1813. The examiner can normally be reached on M-TH (7:00-5:30) Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANH Q. TRAN
PRIMARY EXAMINER

5/25/05